

Remarks:

Reconsideration of the application is requested.

Claims 1-17 remain in the application. Claims 1-6 have been amended. Claims 14-17 have been withdrawn from consideration at this time.

In the section entitled "Claim Rejections - 35 USC § 102" on pages 2-4 of the above-mentioned Office action, claims 1-7, 9, and 11-13 have been rejected as being anticipated by Noble et al. (US Pat. No. 5,973,356) under 35 U.S.C. § 102(b); claims 1-7 and 11-12 have been rejected as being anticipated by Bertin et al. (US Pat. No. 5,468,663) under 35 U.S.C. § 102(b).

The rejections have been noted and claim 1 has been amended in an effort to even more clearly define the invention of the instant application. Support for the changes is found in the drawings and original claim 14.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful.

Claim 1 calls for, inter alia:

a control layer trench formed in the charge storage layer and defined by walls;

a second dielectric layer formed at least partially on the walls of the control layer trench and having a surface; and

a third dielectric layer formed on the surface of the trench extension. (Emphasis added by Applicant).

According to the invention of the instant application, a deep trench is formed in the substrate (20) and reaches as far as the base layer or drain region (1). The upper part of the depression forms a trench (5), while the lower part thereof constitutes a trench extension (5'). A first dielectric layer (8), which acts as a tunnel layer, is formed on the surface of the trench (5). The trench (5) is then filled with a charge storage layer (9), which is subsequently etched to form a control layer trench (5'') therein. Alternatively, the control layer trench (5'') can be formed by coating the side walls of the trench (5) with the charge storage layer (9). The control layer trench (5'') can extend to the bottom of the trench (5) (see Fig. 2), partially into the charge storage layer (9) (see Fig. 3), into the filler material (7) (see Fig. 4), or through the charge storage layer (9) and the filler material (7) into the base layer (1) beneath the trench extension (5') (see Fig. 5). A second dielectric layer (10) is formed on the side walls of the control layer trench (5''). A third dielectric layer (6) is formed on the side walls of the trench extension (5').

Neither Noble et al. nor Bertin et al. disclose a control layer trench and a third dielectric layer formed on the side walls of the trench extension. The layers 515, 520 in Noble et al. and the layer 50 in Bertin et al., identified by the Examiner as the third dielectric layer, are not formed on the surface of the trench extension, rather on the upper surface of the substrate.

Clearly, none of the references shows "a control layer trench formed in said charge storage layer and having walls; a second dielectric layer formed at least partially on said walls of said control layer trench and having a surface; and a third dielectric layer formed on said surface of said trench extension", as recited in claim 1 of the instant application.

Claim 1 is, therefore, believed to be patentable over the art and since claims 2-7, 9 and 11-12 are dependent on claim 1, they are believed to be patentable as well.

In the section entitled "Claim Rejections - 35 USC § 103" on pages 4-5 of the above-mentioned Office action, claim 8 has been rejected as being unpatentable over Noble et al. or Bertin et al. in view of Hong et al. (US Pat. No. 5,457,061) under 35 U.S.C. § 103(a); claim 10 has been rejected as being unpatentable over Noble et al. or Bertin et al. in view of Gregor et al. (US Pat. No. 6,008,091) under 35 U.S.C. §

103(a); claim 13 has been rejected as being unpatentable over Bertin et al. in view of Bergendahl et al. (US Pat. No. 5,399,516) under 35 U.S.C. § 103(a).

As discussed above, claim 1 is believed to be patentable over the art. Since claims 8, 10, and 13 are ultimately dependent on claim 1, they are believed to be patentable as well.

In view of the foregoing, reconsideration and allowance of claims 1-13 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate a telephone call so that, if possible, patentable language can be worked out.

Please charge any fees which might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,


For Applicants

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RALPH E. LOCHER
REG. NO. 41,947

November 22, 2002
Lerner and Greenberg, P.A.
Post Office Box 2480
Hollywood, FL 33022-2480
Tel: (954) 925-1100
Fax: (954) 925-1101

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Marked-Up Version of the Amended Claims:

Claim 1(amended). A vertical non-volatile semiconductor memory cell, comprising:

a substrate having a surface, a drain region, a channel region and a source region;

a trench [that is] formed in said substrate from said source region to said drain region, said trench formed vertically, essentially perpendicular to said surface of said substrate, said trench having trench walls;

a first dielectric layer [that is] formed essentially on said trench walls;

a charge storage layer for storing charges, said charge storage layer [having a surface and essentially] being formed on said first dielectric layer;

a control layer trench formed in said charge storage layer and defined by walls;

a second dielectric layer [that is] formed at least partially on said walls of said [charge storage layer] control layer trench and having a surface;

a control layer [that is] formed essentially on said surface of [the] said second dielectric layer [and that has a surface];

a trench extension [that is] formed essentially underneath said trench, said trench extension having a surface;

a third dielectric layer [located] formed on said surface of said trench extension; and

a filler material for at least partially filling said trench extension.

Claim 2(amended). The vertical non-volatile semiconductor memory cell according to [patent] claim 1, wherein said filler material is electrically isolated from said charge storage layer.

Claim 3(amended). The vertical non-volatile semiconductor memory cell according to [patent] claim 1, wherein said filler material is in electrical contact with said charge storage layer.

Claim 4(amended). The vertical non-volatile semiconductor memory cell according to claim 1, wherein said [second dielectric layer and said control layer extend at least partially] control layer trench extends within said trench.

Claim 5(amended). The vertical non-volatile semiconductor memory cell according to claim 1, wherein said [second dielectric layer and said control layer extend at least partially within said trench and] control layer trench extends into said trench extension.

Claim 6(amended). The vertical non-volatile semiconductor memory cell according to claim 1, wherein said [second dielectric layer and said control layer extend at least partially within said trench, said trench extension and] control layer trench extends into said substrate beneath said trench extension.

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